Analysis of 4H-SiC IGBT Switching in the Presence of Interface Traps using Miller Plateau Characteristics

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Abstract

4H-SiC IGBT characteristics have been investigated based on the carrier trap influence on the switching loss. Special focus is given on the Miller plateau observed in the internal gate voltage. The plateau is enhanced with respect to both height and length under the presence of measured interface traps in the MOSFET channel, even if the deep trap states are successfully eliminated. It is observed that the switching loss can increase by more than 30% due to the shallow trap states. The presence of deep trap also contributes to the loss increase.

1. Introduction

The next generation high-power IGBT device employs the trench-type structure to scale-down the turn-on, on-state and turn-off power losses as shown in Fig. 1 [1]. For SiC-IGBT, however, the device severely suffers from threshold voltage degradation and high on-resistance which is mainly attributed to the high SiO₂/SiC interface state density \(D_α\). Reported measurements of the \(D_α\) are summarized in Fig. 2 [2-4] where the shallow trap is still dominating. The impact of the defects must be clearly addressed to fully realize the scaling down of device structure. The objective of this work is to investigate the switching loss of a 4H-SiC IGBT using the Miller plateau characteristics. Reported \(D_α\) measurements are modeled and incorporated in the 2D numerical simulation of a SiC-IGBT device following literature [5, 6]. The correlation between the Miller plateau and switching characteristics is investigated for shallow and deep traps to determine the importance of reducing the trap density.

2. SiC-IGBT Device Simulation

The simulated \(I-V\) characteristics of a 4H-SiC IGBT after modeling the measured shallow trap is shown in Fig. 3. The subthreshold slope is degraded in the presence of the shallow trap. The probability of carrier trapping, described by capture cross-section parameter \(σ\), is fixed to a typical value of 1e-15. This value determines the trap response characteristics. The device considered is a trench-type IGBT with \(p\)-type channel doping of \(5\times10^{17}\) cm\(^{-3}\) and \(n\)-type base doping of \(8\times10^{11}\) cm\(^{-3}\). The test circuit is shown in Fig. 4.

3. Switching Simulation Results and Discussion

Fig. 5(a) shows the switching characteristics with the measured traps, where the results without trap are compared. It is seen that the Miller plateau of the gate-emitter voltage \(V_{ge}\) is strongly influenced by the traps. The plateau is due to the charging of the gate-collector capacitance \(C_{gc}\) in the gate overlap region. The plateau signifies that the channel is formed and collector current flows as seen in the transient characteristics. The plateau appears as \(V_{ce}\) moves towards zero voltage.

Fig. 5(b) shows the calculated switching loss, with and without traps. More than 30% increase is observed due to the existence of traps. This large increase of the switching loss is attributed to the change in accumulated charges of the overlap region that contributes to charging \(C_{gc}\).

The node potential in the overlap region, depicted by the red dot in Fig. 6, varies strongly according to the amount of charge in the gate \(Q_g\). This internal node potential acts as the drain voltage of the MOSFET and controls the MOSFET current. Changes in the node potential are induced also by the changes in the charges within the overlap region. Trapped carriers due to the traps contribute to these changes.

The presence of carrier trapping increases the height of the plateau as observed in Fig. 5(a). The bigger the capture cross-section \(σ\), the greater the height produced. The formation of the inversion charge in the channel is impeded by the presence of traps especially near the overlap region. As can be seen in Fig. 7, the electron concentration is greater without traps, and thus charging of \(C_{gc}\) is easily accomplished. The presence of traps takes a longer time to charge the channel, and results to a longer plateau. With traps, the switching of collector current \(I_c\) is also delayed which is due to the subthreshold slope degradation as seen in Fig. 3.

The effect of deep (D1) and shallow (D2) traps from another \(D_α\) measurement in Fig. 2(a) on the Miller plateau is shown in Fig. 8. The capture cross-section is again fixed to 1e-15. From the \(V_{ce}\) plot in Fig. 9(a), both trap states are responsible for the switching loss as calculated in Fig. 9(b). The deep trap adds to the loss even though the density is much smaller.

4. Summary

Simulation-based investigation of the Miller plateau characteristics shows that the plateau size increases for a 4H-SiC IGBT under the presence of defects, which is the origin of the carrier traps. Aside from subthreshold degradation, the carrier traps also degrades the potential response at the overlap region. Accumulation of charges in the overlap region modifies the gate-collector capacitance which enhances the Miller plateau. Switching loss increases by more than 30%, caused mainly by the shallow trap states.
References

Fig. 1. Power loss of Si IGBT in an inverter.

Fig. 2. (a) Reported measurements of interface defect densities. (The dashed line is used for the simulation.) (b) I-V degradation due to D1 and D2 traps [5].

Fig. 3. Degradation of I-V characteristics with measured shallow traps (dashed line in Fig. 2(a)). The shallow trap causes wide degradation across the gate voltage.

Fig. 4. Transient test circuit.

Fig. 5(a) Miller plateau and device switching characteristics without and with traps. The measured shallow (trap dashed line in Fig. 2(a)) is used. (b) Calculated switching loss.

Fig. 6. Schematic illustration of IGBT with the node potential, depicted by the red dot, that determines the MOSFET drain voltage and at the same time the overlap region characteristics.

Fig. 7. Electron concentration (a) without and (b) with traps at \( t=61.5 \mu s \). With the presence of traps the concentration is decreased because carriers traversing the channel are impeded.

Fig. 8. Effect of shallow and deep traps on the collector voltage using \( D1 \) and \( D2 \) in Fig. 2(a).

Fig. 9. (a) Effect of shallow and deep traps on the Miller plateau using \( D1 \) and \( D2 \) in Fig. 2(a). (b) Calculated switching loss.